Delta-Sigma Modulator with Bandwidth 100kHz and SNR 120 dB

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ABSTRACT

The paper presents a modeling and simulation of third-order tri-level cascade-of-multiple-feedback (CIFB) delta sigma modulator which is an Analog to Digital Converter (ADC) for signal bandwidth 100 kHz with oversampling ratio of 128. It can attain signal to noise ratio of 120dB. The Out of Band Gain of the modulator is lowered for higher stability while keeping the full scale smaller with 850mV. The noise transfer function (NTF) shows 3rd order noise shaping with roll off 60dB/decade. The signal transfer function (STF) shows flat at low frequencies and decreased at higher frequencies. The loop filter integrators are optimized for higher gain for maximum performance of the modulator. The modulator uses oversampling ration of 128 for the signal bandwidth of 100 kHz. The three-feedback digital-to-analog (DAC) provides the stability to the loop filter. The larger swing inside the loop filter demands higher DC gain amplifier. The NTF zero optimization is implemented for further reduction of in-band noise to enhance the SNR. The proposed modulator topology utilizes OBG of 1.5 and with NTF zero optimization can achieve SNR of 120 dB with OSR of 128 for full-scale input signal of 850 mV. The operational amplifier performance parameters like slew-rate, gain bandwidth, DC gain investigated for optimized performance. Finally, this proposed modulator can achieve SNR equal to 120 dB for signal of bandwidth 100 kHz.

Keywords: out-of-band gain, Signal-transfer function, Noise transfer function, Digital-to-analog converter, Operational amplifier.

1. INTRODUCTION

Digital electronics, wireless communication, and integrated sensors are the basic building block for low power, low cost, functional portable sensor systems as required for broad range of applications. Data converter are, main building block of this structure which most of the time use resolutions in 8 to14 bit range while signal bandwidth is from 50 to 150 kHz and the power dissipation is very low. Analog to digital converters based on successive approximation register receive very low power up to 10 to 12 bits. To obtain resolutions greater than 12 bits, trading on noise shaping and oversampling [9] can result in efficient use of low power. These circuits can attain low power by the complete selection of the amount of oversampling size & the no. of quantizer bits. In addition, it's possible to reduce power dissipation by using the no. of op-amps lower than the module system. The 2nd order modulator is seen with only 1 op amp and the 3rd order modulator used with 2 op amps, respectively. The third order DSM for 3rd order is investigated with a 100 kHz signal bandwidth. STF and NTF of modulator are being investigated for high performance resulting in the modulator reaching up to 120dB SNR of 100 kHz signal bandwidth. This work introduces the current input of a continuous sigma-delta modulator for biomedical applications like electrochemical impedance spectroscopy. Low noise and digitizer inputs at lower area current are required to use high spatial adjustment for multiple electrode

arrays. The use of modified capacitor with resistor DAC for current input of a continuous sigma-delta modulator is presented. SCR-DACs offer the fulfillment of high resistance in a small area, resulting in the use of very small area combined with good sound performance. current input of a continuous sigma-delta modulator with capacitor with resistor DAC prototype was performed with a 180nm CMOS process. ADC used takes up only 120 × 200 μm2 space. To maximize dynamic range of current input of a continuous sigma-delta modulator, two modes have been used. In configuration of low noise, 157-pArms is integrated in band noise with frequency in the 100 kHz band with maximum Signal to noise and distortion frequency of 62 dB. In high-resolution DR, a 72 dB SNDR and MSA of -4.1 dB corresponding to 9.1 μA is measured. Complete C-CTΣΔM used 2mW at 3 volt supply and reaches a total of 95 dB DR [1]. The delta-sigma module delta-sigma for the third order of low power switch is defined. Architecture uses one operating amplifier that works in timely manner. The structures use swing reduction method to minimize swing and the execution needs of all internal nodes. Available with 0.18- m 2P6M CMOS technology, the modulator offers 84-dB SNDR and 88-dB flexible bandwidth at 100 kHz signal bandwidth and a clock in 3.2MHz. A given 1.5 volt prototype consumes 140 W with FoM 54 fJ / conversion rate [2]. This proposed a low high- resolution band pass Delta sigma ADC for accelerometer applications. A high performance 6^{th} order feedforward modulator with 1 bit quantization and low-power, area efficient digital filter comprises presented band pass ADC. The ADC is created in a 180nm with 1P6M mixed signal CMOS technology with a 5 mm^2 device size. Over a 4 kHz bandwidth, proposed high resolution ADC has acquired 90 dB peak signal to noise plus distortion ratio and DR of 96 dB, while this intermediate frequency (IF) is moving from 100 KHz to 200 KHz. The chip's power dissipation is 5.6 mW when powered by a 1.8 V (digital)/3.3 V (analogue) supply [3].

The modelling and simulation of a third-order tri-level cascade-of-multiple-feedback (CIFB) delta-sigma modulator were established in this study. An ADC having a signal bandwidth of 100 kHz and an OSR of 128 will obtain a signal to noise ratio of 120dB. The modulator's out-of-band-gain (OBG) is reduced for more stability while preserving the whole scale at 850mV. The noise transfer function (NTF) demonstrates 3^{rd} order noise shaping with roll-off of 60dB/decade. The signal transfer function (STF) is flat at low frequencies and decreases as frequency increases. For best modulator performance, the loop filter integrators are adjusted for greater gain. The modulator use an oversampling ratio of 128 while Signal bandwidth is 100KHz. The loop filter's stability is provided by a three-feedback digital-to-analog (DAC). The increased swing within the loop filter needs a larger DC gain amplifier. The Noise transfer function zero optimization is used to further minimize in band noise and improve SNR. The presented modulator architecture uses OBG of 1.5 and can reach SNR of 120 dB with OSR of 128 for a full-scale input signal of 850 mV with NTF zero optimization. For optimal performance, operational amplifier performance characteristics such as slew-rate, gain bandwidth, and DC gain were examined. Finally, given a signal bandwidth of 100 kHz, the modulator can attain SNR of 120 dB.

After the introduction, the second section discuss the design of the modulator design with CIFB and CIFF structure, while the third section describes the modeling and simulation of the modulator and explain the operational amplifier for integrator for the fifth-order 4-bit quantizer for CT design implementation. Finally, the section four concludes the paper

2. MODULATOR DESIGN

A third order with three integrators in the loop filter and tri-level quantizer modulator modeled using Delta-Sigma Toolbox [12]. The cascade integrator with multiple feedback (CIFB) investigated for much lower out of band gain of 1.5 for higher stability with oversampling ratio of 128 with NTF zero optimization technique. The modulator with CIFB topology can achieve SNR of 120 dB with OSR of 128. Due to the reason of low pass modulator, the STF of the modulator have low pass behavior. While the NTF have high pass response to shape more quantization noise at high frequency. The third order modulator OBG of 1.5 is shown in Figure 1. The STF also shown as low pass filter. The NTF zeroes, and STF zeroes also shown in the Figure 2. The loop filter poles also plotted and shown in Figure 2. The signal transfer function and noise transfer function of the modulator is shown in Figure 1. As it is shown from the Figure 1 clearly that the OBG of the CIFB modulator is 1.5. While STF of the modulator shows low-pass response to allow those signals, which are at low frequencies and attenuate high frequency signal. The Figure 2 shows NTF and STF plot, as the modulator is low-pass, so the STF shows the low-pass response, while the NTF shapes the quantization noise at high frequencies. Figure 3 shows the output PSD plot with SNR of 120, achieving ENOB of 19-bit. The modulator NTF shows a sharp noise shaping response due to the

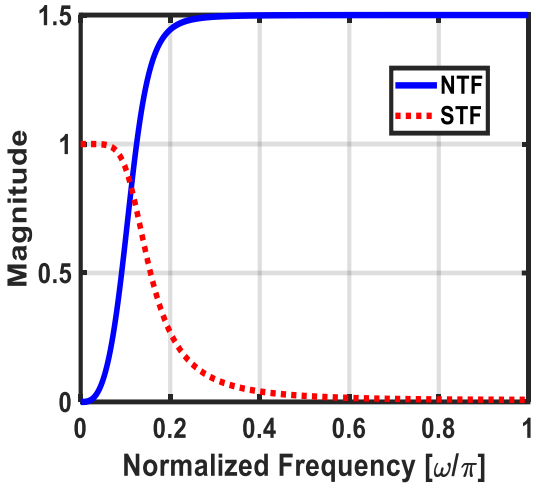

Figure 1: STF and NTF plot (CIFB)

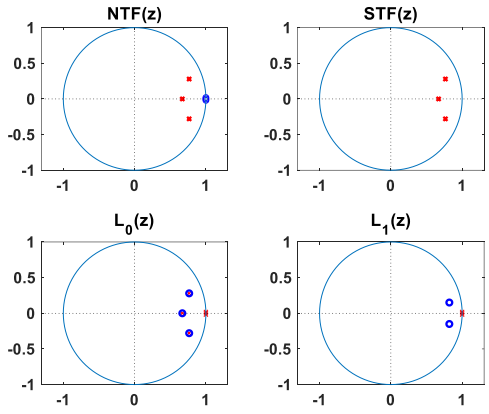

Figure 2: STF and NTF plot (CIFB)

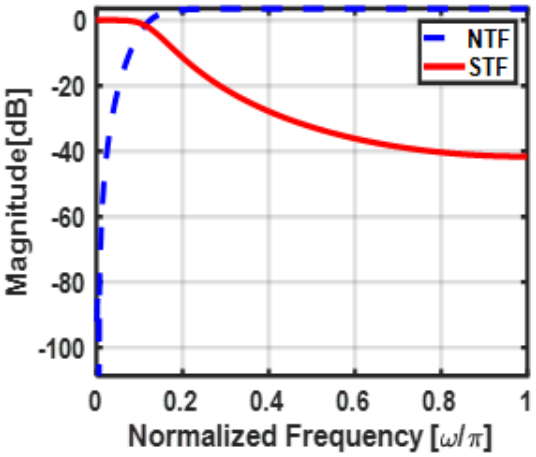

Figure 3: STF and NTF plot (CIFB)

reason that all integrator inside the loopfilter is assumed having infinite DC

gain. The noise floor is at the level of -140dB, the quantization noise is suppressed maximum with three integrators inside the loop filter. Due to moderate OSR of 128, the signal bandwidth is quite small. Due to CIFB topology of the modulator the signal swing inside the loop filter is large as a results operational amplifier with very high DC gain will be demanded for the suppression of the quantization noise. Due to CIFB topology the stability of the loop filter is very high due to the advantage of multiple feedbacks, while the overall modulator becomes power hungry with many high DC gain amplifier inside the loop filter.

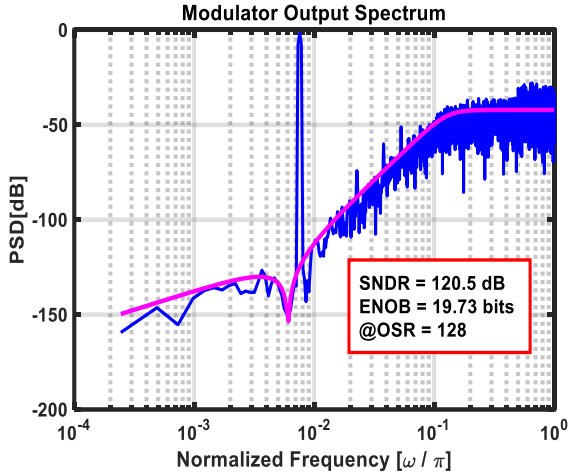

Figure 4: Output PSD plot (CIFB)

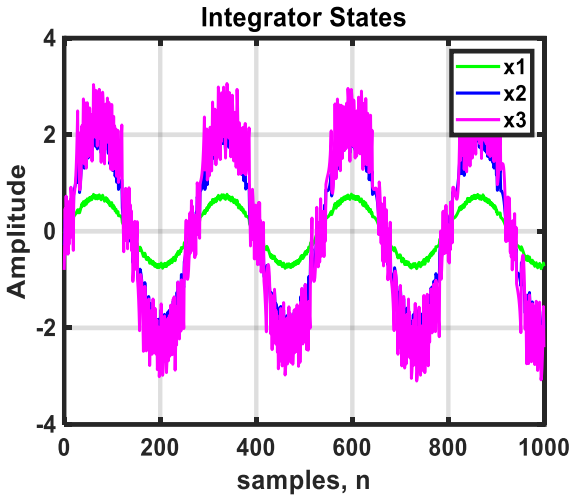

Figure 5: Output states of the integrators

3. RESULTS & DICUSSION

The third-order single-bit modulator simulated and modeled in MATLAB for signal bandwidth of 100 kHz for SNR of 120 dB with input signal of 850 mV. The operational amplifier performance investigates for slew-rate, gain bandwidth, DC gain. The simulation environment SD Toolbox [14] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

4. CONCLUSION

A high-resolution delta-sigma modulator modeled for signal bandwidth of 100 kHz with SNR of 120 dB. The operational amplifier inside the integrator is investigated for limited gain bandwidth, slew-rate and DC gain. The out-of-band-gain (OBG) of the modulator is lowered for higher stability while keeping the full scale smaller with 850mV. The noise transfer function (NTF) shows third-order noise shaping with roll off 80dB/decade. The signal transfer function (STF) shows flat at low frequencies and decreased at higher frequencies. The loop filter integrators are optimized for higher gain for maximum performance of the modulator. The modulator uses oversampling ration of 128 for the signal bandwidth of 100 kHz. The three-feedback digital-to-analog (DAC) provides the stability to the loop filter. The larger swing inside the loop filter demands higher DC gain amplifier. The NTF zero optimization is implemented for further reduction of in-band noise to enhance the SNR. The proposed modulator topology

utilizes OBG of 1.5 and with NTF zero optimization can achieve SNR of 120 dB with OSR of 128 for full-scale input signal of 850 mV. The operational amplifier performance parameters like slew-rate, gain bandwidth, DC gain investigated for optimized performance. Finally, the modulator can accomplish SNR of 120 dB for signal bandwidth equal to 100 kHz.

5. ACKNOWLEDGMENT

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